Capacitor-Free, 150-mA, Low-Dropout Regulator with Foldback Current Limit for Portable Devices

Check for Samples: TLV713, TLV713P

FEATURES

- **Very Low Dropout: 250 mV at 150 mA**
- **Accuracy: 1%**
- **Low I_Q: 50 µA**
- **Input Voltage Range: 1.4 V to 5.5 V**
- **Available in Fixed-Output Voltages: 1.0 V to 3.6 V**
- **High PSRR: 70 dB at 1 kHz**
- **Stable Operation With or Without Capacitors**
- **Foldback Overcurrent Protection**
- **Package: SOT23-5, DFN, and DPW**

APPLICATIONS

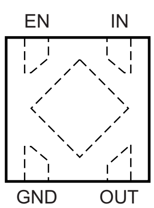
- **PDAs and Battery-Powered Portable Devices**
- **MP3 Players and Other Hand-Held Products**
- **WLAN and Other PC Add-On Cards**

DESCRIPTION

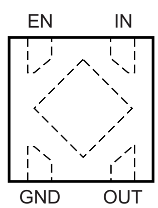
The TLV713 series of low-dropout (LDO) linear regulators are low quiescent current LDOs with excellent line and load transient performance and are designed for power-sensitive applications. These devices provide a typical accuracy of 1%.

The TLV713 series is available in standard DQN, DPW, and DBV packages. The TLV713P provides an active pull-down circuit to quickly discharge output loads.

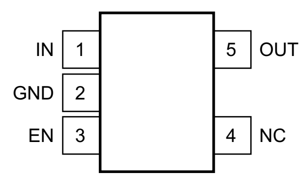
DQN Package
1-mm x 1-mm DQN
(Top View)



DPW Package
0,8-mm x 0,8-mm DQN
(Top View)



DBV PACKAGE
SOT23-5
(Top View)



NOTE: DPW and DBV versions are Product Preview devices.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)(2)

PRODUCT	V_{OUT}
TLV713**xx(x)Pyyyz**(3)	**XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 475 = 4.75 V). **P** is optional; devices with P have an LDO regulator with an active output discharge. **YYY** is the package designator. **Z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.0 V to 3.3 V in 50-mV increments are available. Contact the factory for details and availability.
(3) DPW and DBV versions are Product Preview devices.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –25°C, unless otherwise noted. All voltages are with respect to GND.

		VALUE		UNIT
		MIN	MAX	
Voltage	Input range, V_{IN}	–0.3	6.0	V
	Enable range, V_{EN}	–0.3	V_{IN} + 0.3	V
	Output range, V_{OUT}	–0.3	6.0	V
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Total power dissipation	Continuous, P_{DISS}	See Thermal Information table		
Temperature	Junction range, T_J	–55	+85	°C
	Storage junction range, T_{stg}	–55	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)		2000	V
	Charged device model (CDM)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TLV713xx TLV713xxP			UNITS
		DQN (DFN)	DPW (DQN)	DBV (SOT23)	
		4 PINS	4 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	255.8	249.4	TBD	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	159.3	183.4	TBD	
θ_{JB}	Junction-to-board thermal resistance	208.2	203.5	TBD	
ψ_{JT}	Junction-to-top characterization parameter	16.2	14.5	TBD	
ψ_{JB}	Junction-to-board characterization parameter	208.1	203.3	TBD	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	148.6	152.5	TBD	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

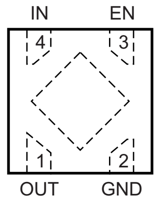
At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{OUT} = 0.47 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TLV713 MIN	TLV713 TYP	TLV713 MAX	UNIT
V_{IN}	Input voltage range			1.4		5.5	V
V_{OUT}	Output voltage range			1.0		3.6	V
	DC output accuracy	V_{OUT} ≥ 1.8 V, T_A = +25°C		–1		1	%
		V_{OUT} < 1.8 V, T_A = +25°C		–20		20	mV
		V_{OUT} ≥ 1.2 V, –40°C ≤ T_A ≤ +85°C		–1.5		1.5	%
		V_{OUT} < 1.2 V, –40°C ≤ T_A ≤ +85°C		–50		50	mV
$\Delta V_O/V_{IN}$	Line regulation				1	5	mV
$\Delta V_O/I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA			10	30	mV
V_{DO}	Dropout voltage	V_{OUT} = 0.98 × $V_{OUT(NOM)}$	1.8 V ≤ V_{OUT} < 2.1 V, I_{OUT} = 30 mA		110		mV
			1.8 V ≤ V_{OUT} < 2.1 V, I_{OUT} = 150 mA		330	575	mV
			2.1 V ≤ V_{OUT} < 2.5 V, I_{OUT} = 30 mA		90		mV
			2.1 V ≤ V_{OUT} < 2.5 V, I_{OUT} = 150 mA		280	400	mV
			2.5 V ≤ V_{OUT} < 3.0 V, I_{OUT} = 30 mA		80		mV
			2.5 V ≤ V_{OUT} < 3.0 V, I_{OUT} = 150 mA		250	350	mV
			3.3 V ≤ V_{OUT} < 3.6 V, I_{OUT} = 30 mA		75		mV
			3.3 V ≤ V_{OUT} < 3.6 V, I_{OUT} = 150 mA		230	420	mV
I_{GND}	Ground pin current	I_{OUT} = 0 mA			50	75	µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 4.5 V, T_A = +25°C			0.1	1	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 30 mA	f = 100 Hz		70		dB
			f = 10 kHz		55		dB
			f = 1 MHz		55		dB
V_{NOISE}	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			55		μV_{RMS}
t_{STR}	Startup time(1)	C_{OUT} = 1.0 µF, I_{OUT} = 150 mA			100		µs
V_{HI}	Enable high (enabled)			0.9		V_{IN}	V
V_{LO}	Enable low (disabled)			0		0.4	V
I_{EN}	EN pin current	EN = 5.5 V			0.01		µA
$R_{PULLDOWN}$	Pull-down resistor (TLV713P only)	V_{IN} = 4 V			120		Ω
T_J	Operating junction temperature			–40		+125	°C
I_{LIM}	Output current limit	V_{IN} = 3.8 V, V_{OUT} = 3.3 V		180			mA
		V_{IN} = 2.25 V, V_{OUT} = 1.8 V		180			mA
		V_{IN} = 2.0 V, V_{OUT} = 1.2 V		180			mA
I_{SC}	Short-circuit current	V_{OUT} = 0 V			40		mA
T_{SD}	Thermal shutdown	Shutdown, temperature increasing			158		°C
		Reset, temperature decreasing			140		°C
V_{DO}	Dropout voltage	V_{OUT} = 0.98 × $V_{OUT(nom)}$			590	900	mV

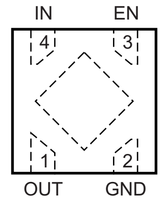
(1) Startup time is the time from EN assertion to (0.98 × $V_{OUT(nom)}$).

PIN CONFIGURATION

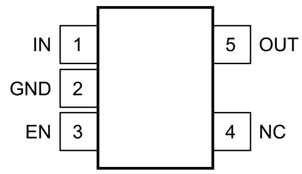
DQN PACKAGE
1-mm × 1-mm DFN
(Top View)



DPW PACKAGE
0,8-mm × 0,8-mm DQN
(Top View)



DBV PACKAGE
SOT23-5
(Top View)



PIN DESCRIPTIONS

PIN			
NAME	DQN, DPW	SOT23-5	DESCRIPTION
EN	3	3	Enable pin. Driving EN over 1.2 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
GND	2	2	Ground pin
IN	4	1	Input pin. A small capacitor is recommended from this pin to ground. See the *Input and Output Capacitor Requirements* section in the *Application Information* for more details.
NC	—	4	No connection
OUT	1	5	Regulated output voltage pin. For best transient response, a small 1-μF ceramic capacitor is recommended from this pin to ground. See the *Input and Output Capacitor Requirements* section in the *Application Information* for more details.
Thermal pad	—	—	TI recommends connecting this pin to GND for improved thermal performance.

FUNCTIONAL BLOCK DIAGRAMS

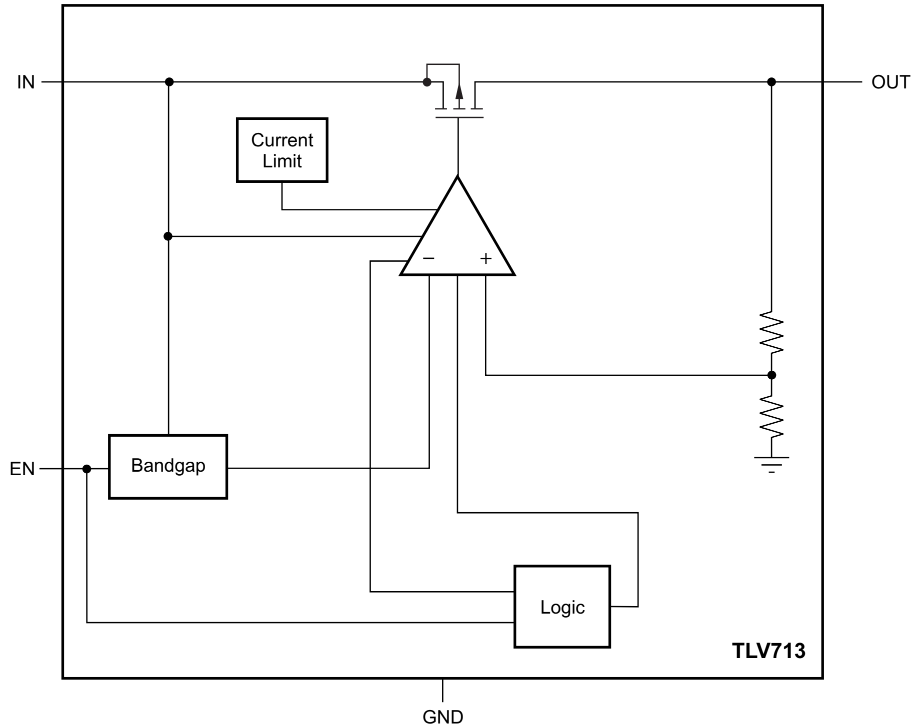


Figure 1. TLV713 Block Diagram

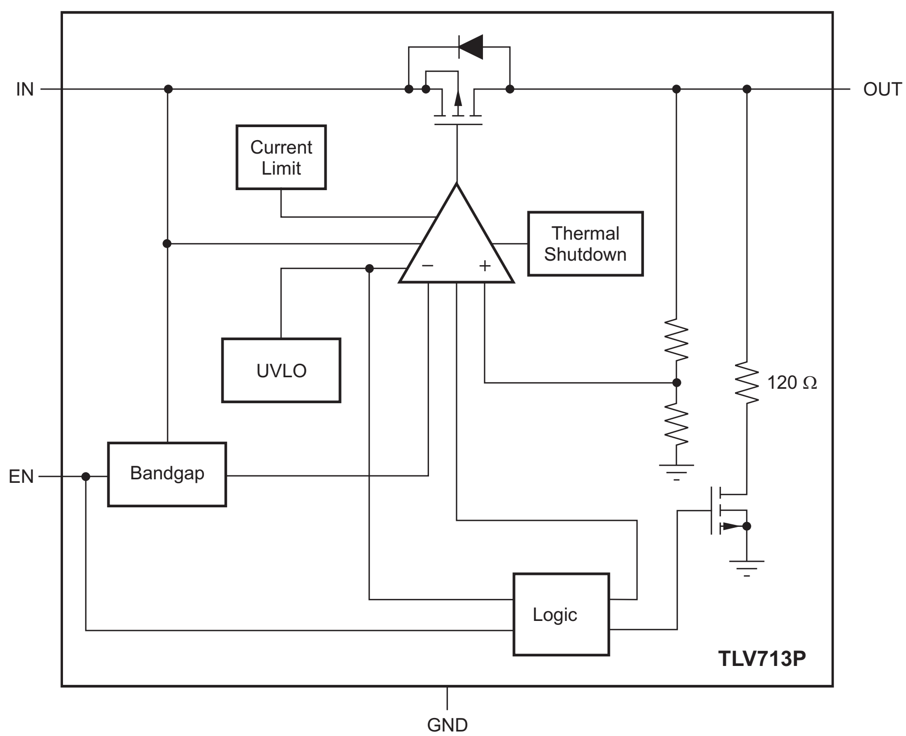


Figure 2. TLV713P Block Diagram

TYPICAL CHARACTERISTICS

At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

APPLICATION INFORMATION

The TLV713 belongs to a new family of next-generation value low-dropout (LDO) regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for RF portable applications.

This family of regulators offers current limit and thermal protection. Device operating junction temperature is –40°C to +125°C.

INPUT AND OUTPUT CAPACITOR CONSIDERATIONS

The TLV713 uses an advanced internal control loop to obtain stable operation both with and without the use of input or output capacitors. The dynamic performance of the TLV713xx is improved with the use of an output capacitor. An output capacitance of 0.1 µF or larger generally provides good dynamic response. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the source impedance is more than 0.5 Ω, a 0.1-µF input capacitor may be necessary to ensure stability. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the input power source.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection should be connected directly to the device GND pin. High ESR capacitors may degrade PSRR performance.

INTERNAL CURRENT LIMIT

The TLV713 has an internal foldback current limit that helps to protect the regulator during fault conditions. The current supplied by the device is gradually throttled down while the output voltage decreases. When the output is shorted, the LDO supplies a typical current of 40 mA. Output voltage is not regulated when the device is in current limit, and is ($V_{OUT} = I_{LIMIT} \times R_{LOAD}$). The PMOS pass transistor dissipates [(V_{IN} – V_{OUT}) × I_{LIMIT}] until thermal shutdown is triggered and the device turns off. While the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details.

The TLV713 PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

SHUTDOWN

The enable pin (EN) is active high. The device is enabled when the voltage at the EN pin goes above 0.9 V. This relatively lower voltage value required to turn the LDO on can be exploited to power the LDO with a GPIO of recent processors whose GPIO logic 1 voltage level is lower than traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

POWERING THE MSP430 MICROCONTROLLER

Figure 3 shows a diagram of the TLV713 powering an MSP430 microcontroller. Several versions of the TPS713 are ideal for powering the MSP430 microcontroller. Table 1 shows potential applications of some voltage versions.

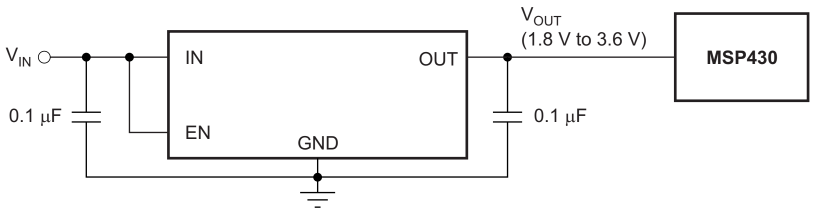


Figure 3. TLV713 Powering a Microcontroller

Table 1. Typical MSP430 Applications

DEVICE	V_{OUT} (Typ)	APPLICATION
TLV71319	1.9 V	V_{OUT}, minimum > 1.8 V required by many MSP430s, allows lowest power consumption operation
TLV71323	2.3 V	V_{OUT}, minimum > 2.2 V required by some MSP430s FLASH operation
TLV71330	3.0 V	V_{OUT}, minimum > 2.7 V required by some MSP430s FLASH operation

DROPOUT VOLTAGE

The TLV713 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 14 of the *Typical Characteristics* section.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

UNDERVOLTAGE LOCKOUT (UVLO)

The TLV713 uses an undervoltage lockout (UVLO) circuit to keep the output shut off until the internal circuitry operates properly.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The TLV713 internal protection circuitry is designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TLV713 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC-low and high-K boards are given in the Thermal Information table. Using heavier copper increases the effectiveness in removing heat from the device. The addition, plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation (P_D) depends on input voltage and load conditions. P_D is equal to the product of the output current and voltage drop across the output pass element, as shown in Equation 1.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (1)$$

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TLV71312PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71312PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71315PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	
TLV71315PDQNT	PREVIEW	X2SON	DQN	4	250	TBD	Call TI	Call TI	
TLV713185PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	
TLV713185PDQNT	PREVIEW	X2SON	DQN	4	250	TBD	Call TI	Call TI	
TLV71318PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71318PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71325PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	
TLV71325PDQNT	PREVIEW	X2SON	DQN	4	250	TBD	Call TI	Call TI	
TLV713285PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	
TLV713285PDQNT	PREVIEW	X2SON	DQN	4	250	TBD	Call TI	Call TI	
TLV71328PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	
TLV71328PDQNT	PREVIEW	X2SON	DQN	4	250	TBD	Call TI	Call TI	
TLV71330PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	
TLV71330PDQNT	PREVIEW	X2SON	DQN	4	250	TBD	Call TI	Call TI	
TLV71333PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71333PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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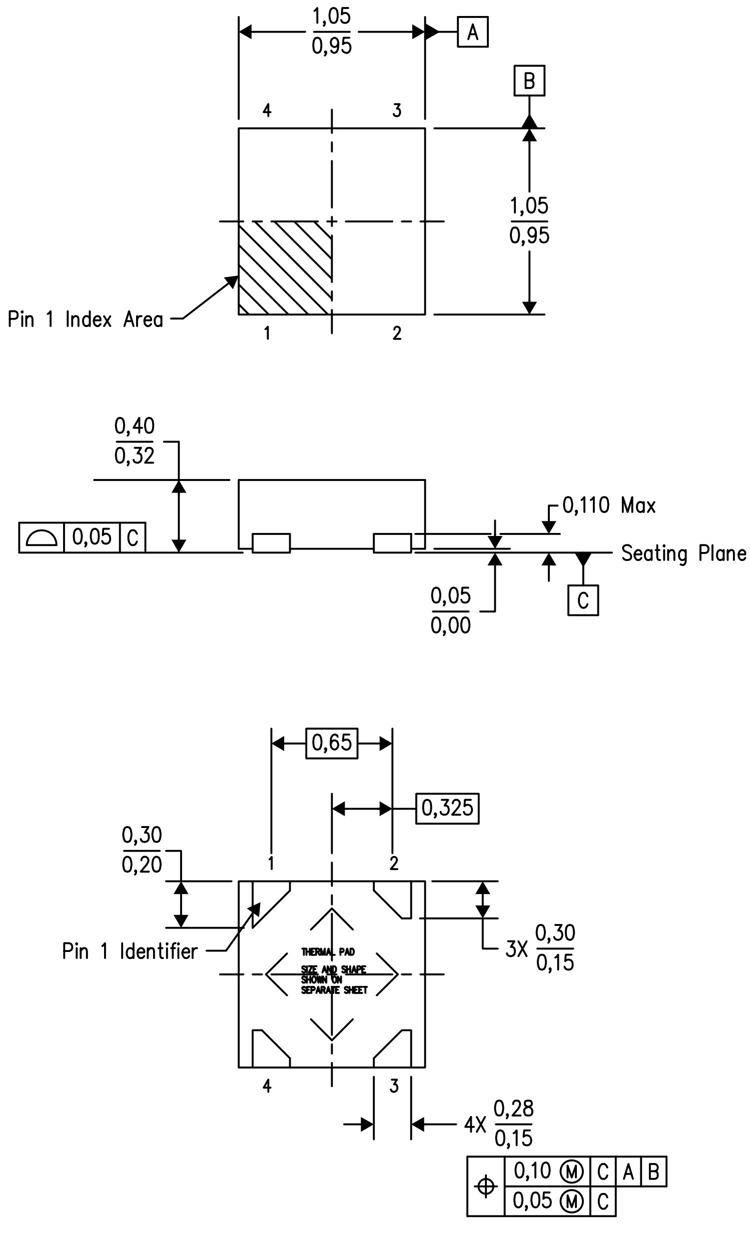
DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

Products		**Applications**	
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